

PG401 A02


4GB GDDR5, 256b, 128Mx32

Tall DVI-I + DP + DP + DP/HDMI + DP

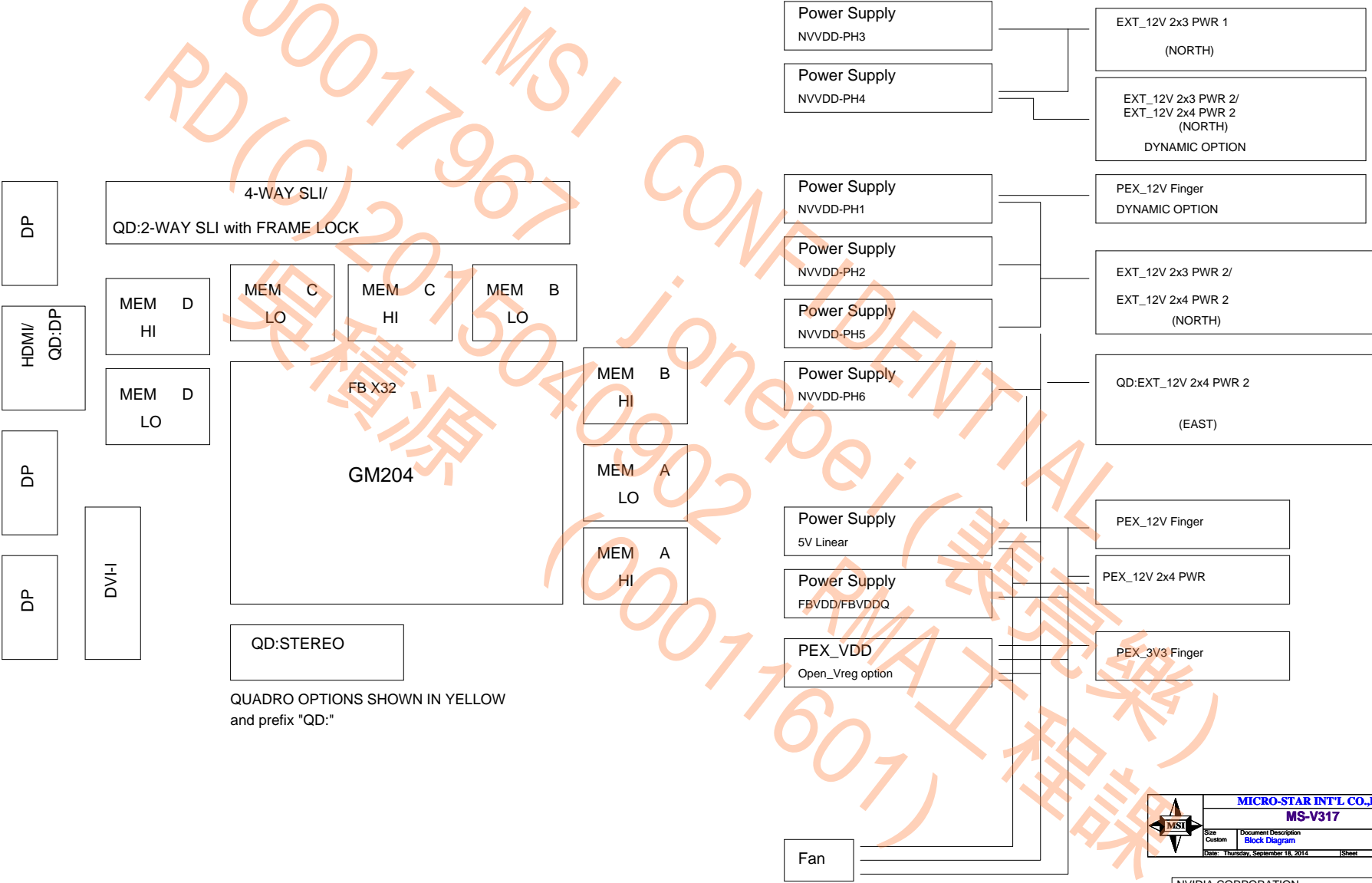
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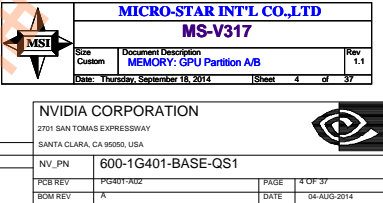
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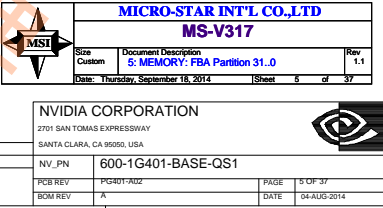
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PAGE DETAIL	Block Diagram

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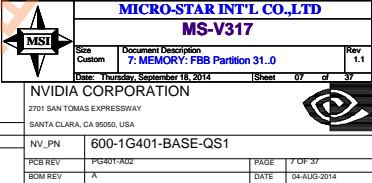


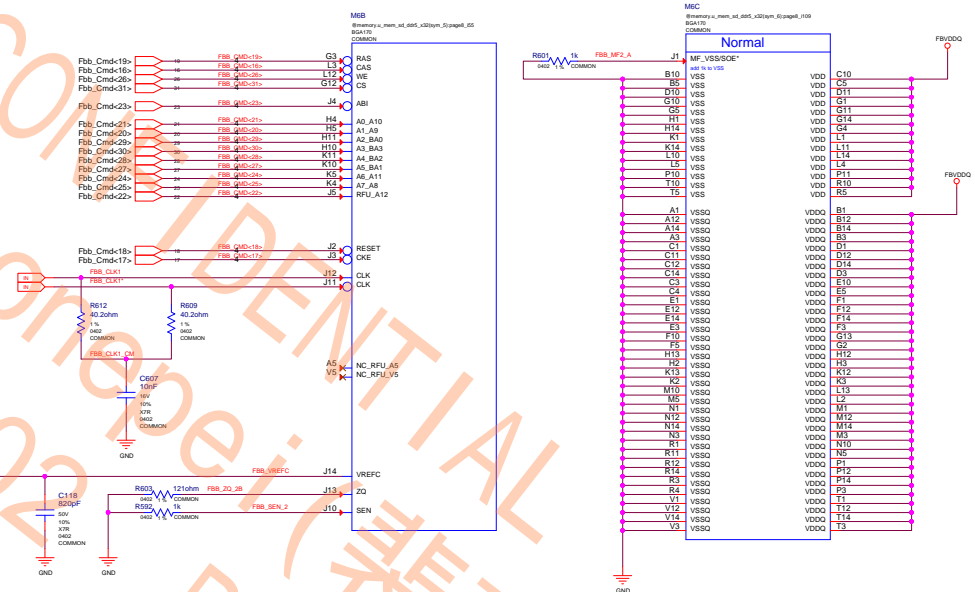
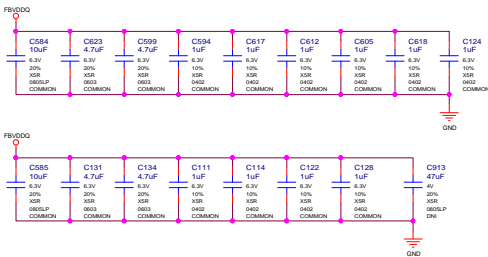
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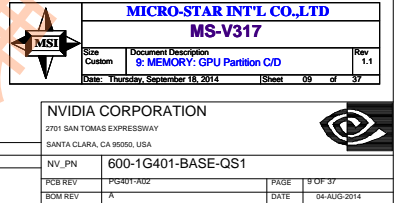


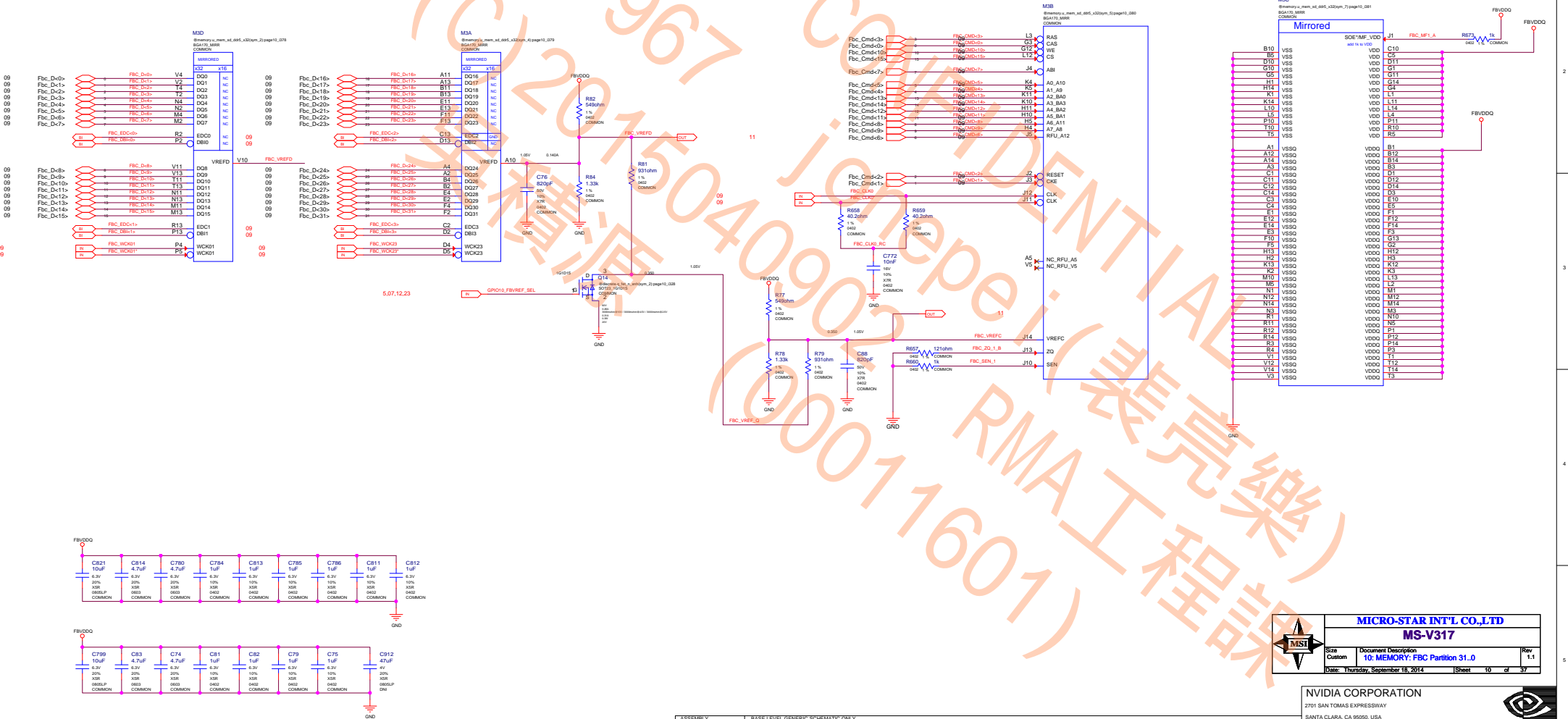
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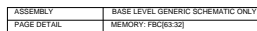
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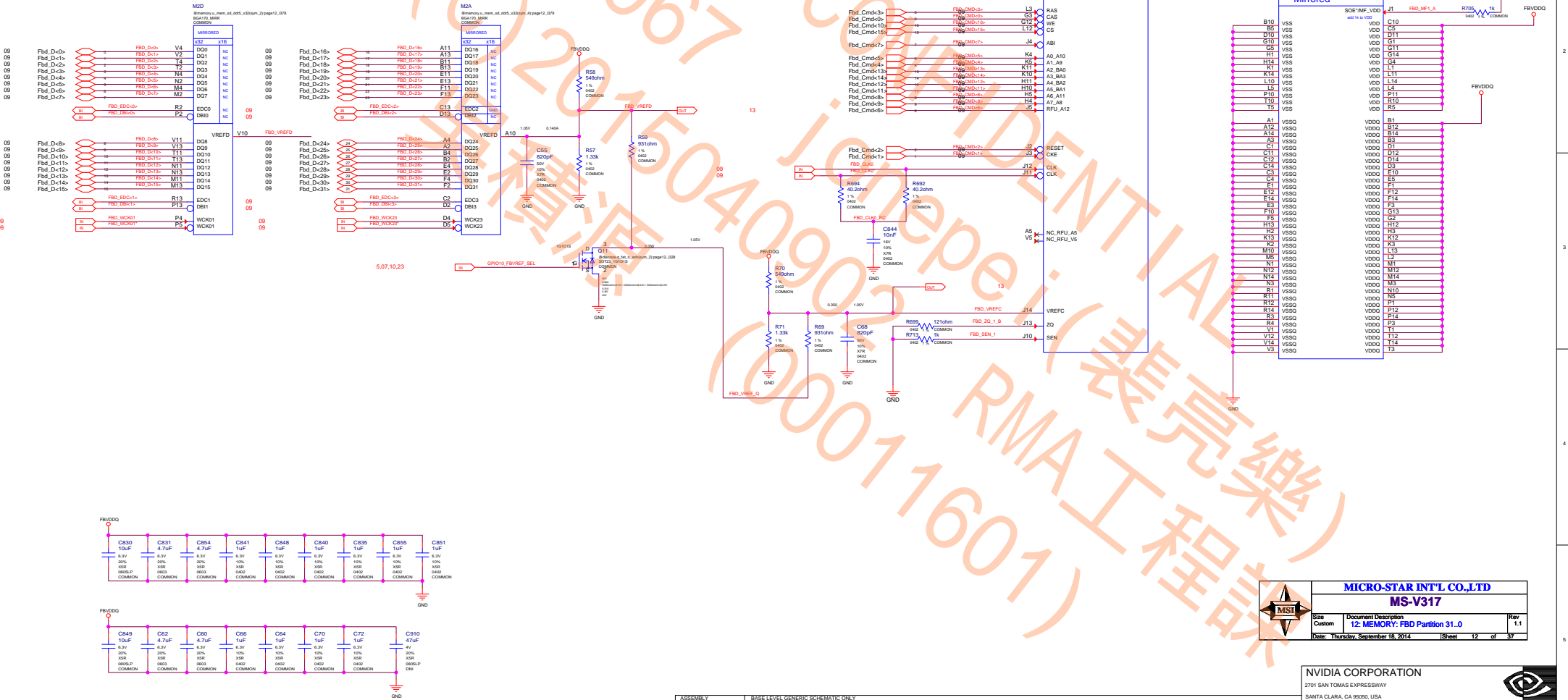
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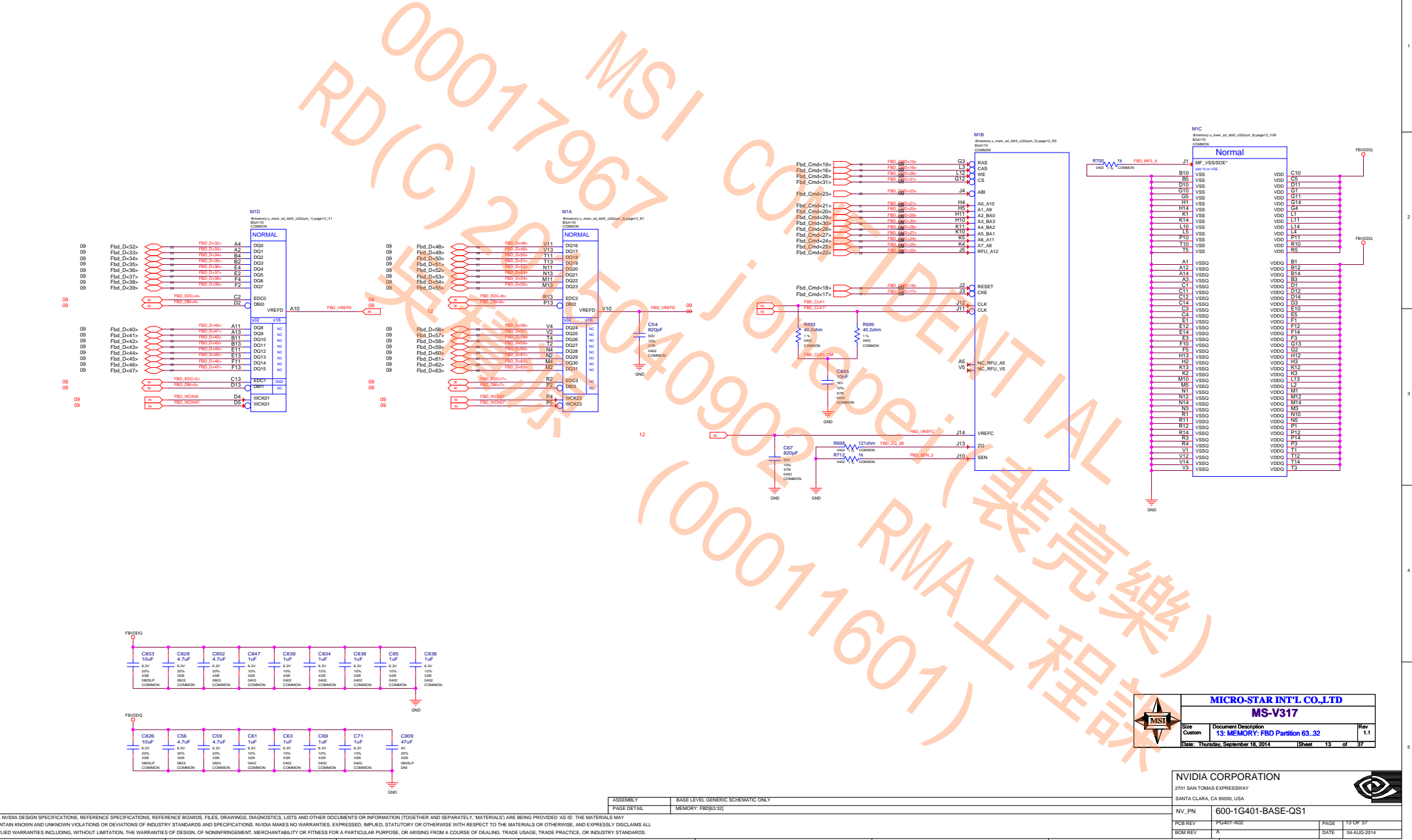
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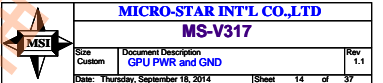
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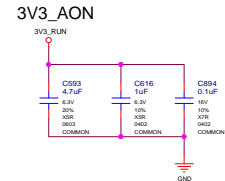
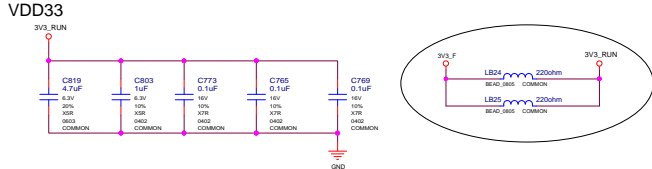
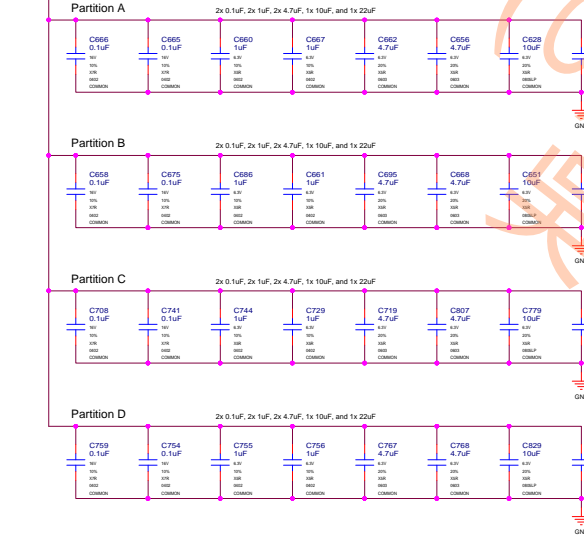
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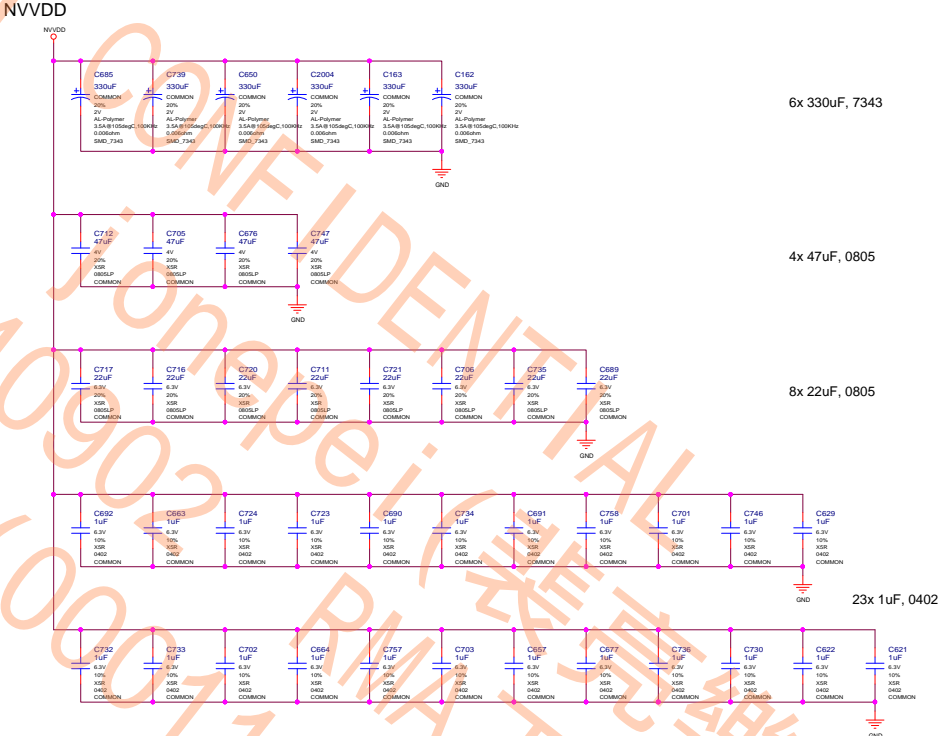
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Based on GB2-X GDDR5 FBVDDQ Decap Guideline

FBVDDQ
0.1uF, 0.47uF & 1uF, 0402 (Place Under GPU)
4.7uF, 0603 (Place Near GPU)
10uF, 0805 (Place Near GPU)
22uF, 0805 (Place Near GPU)



NVVDD Decoupling caps. Place under GPU.



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PAGE DETAIL	GPU Decoupling

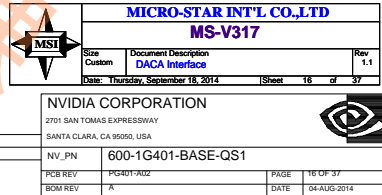
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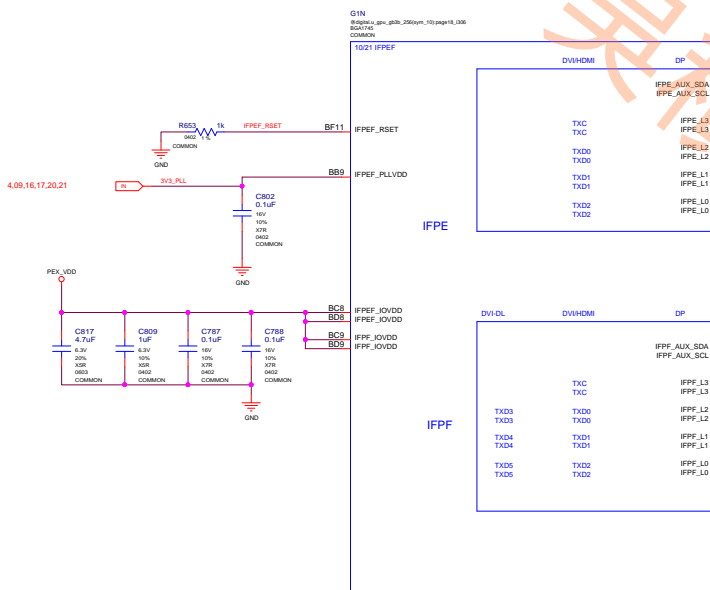
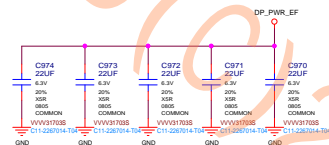
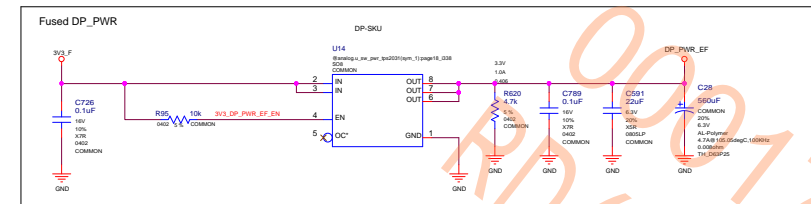


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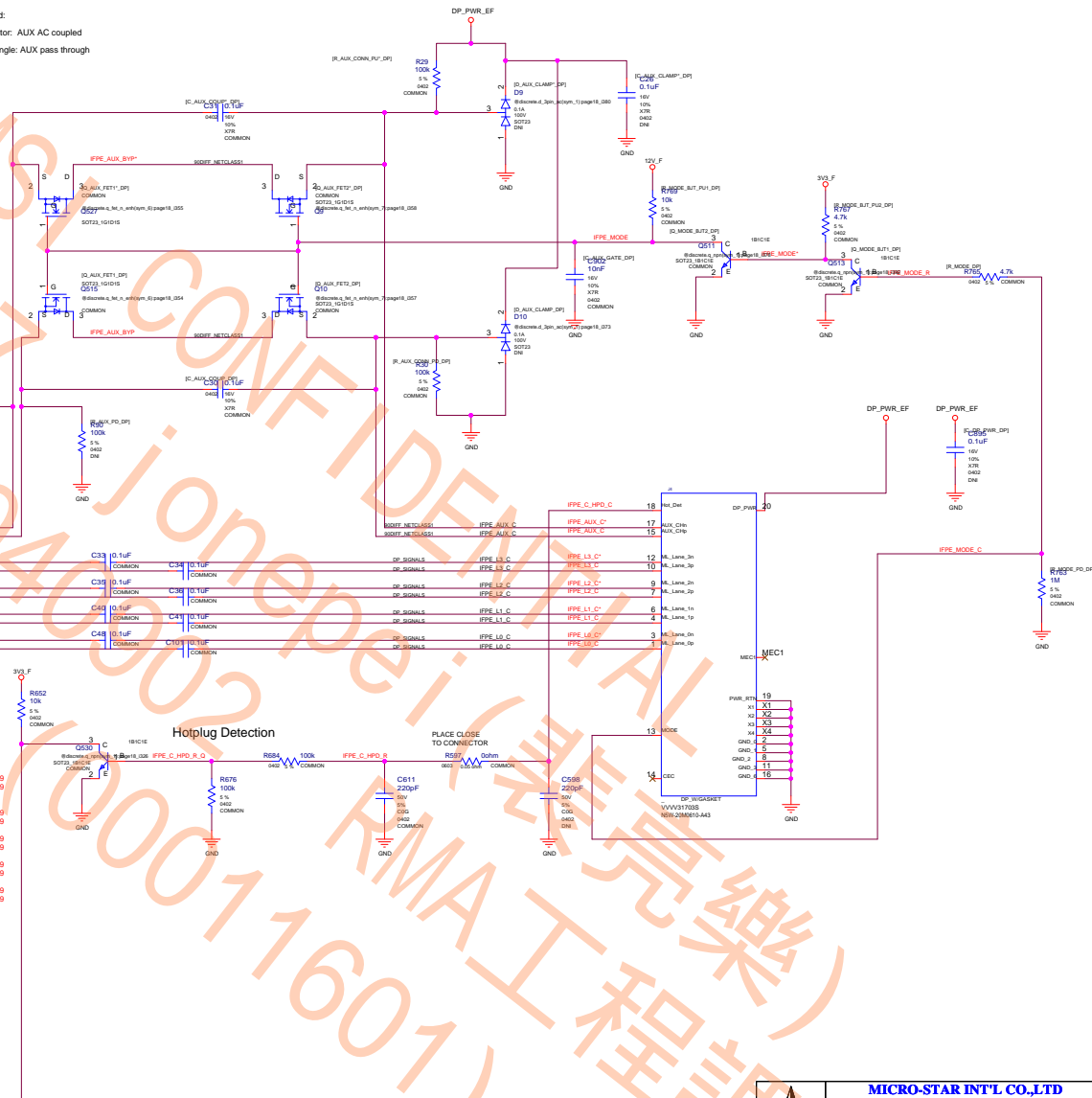


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- Two cases to be considered:
1. DP AUX to DP connector: AUX AC coupled
 2. DP AUX to DP-DVI dongle: AUX pass through



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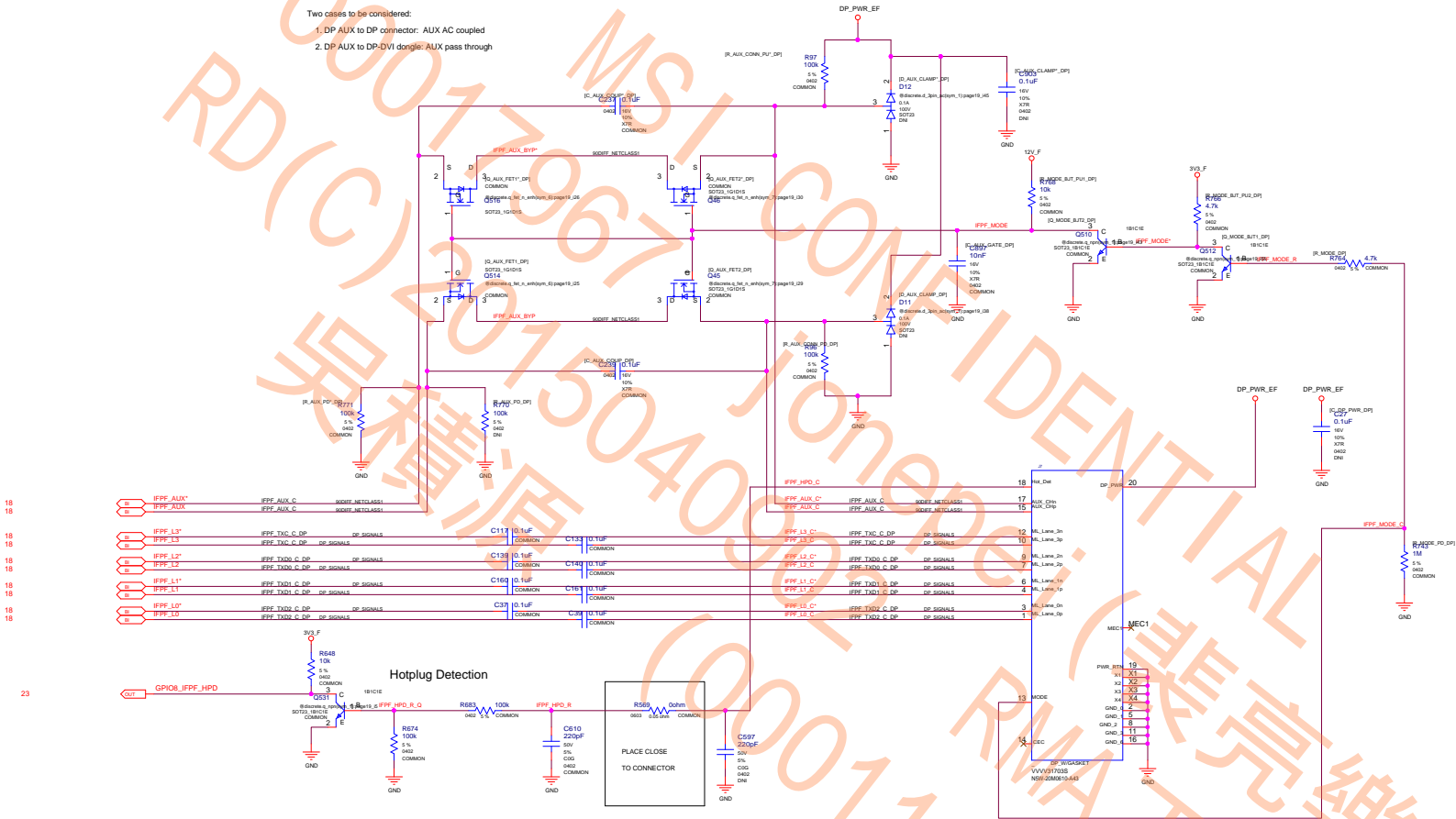
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- Two cases to be considered:
- 1. DP AUX to DP connector: AUX AC coupled
 - 2. DP AUX to DP-DVI dongle: AUX pass through



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PAGE DETAIL	IFPF DP

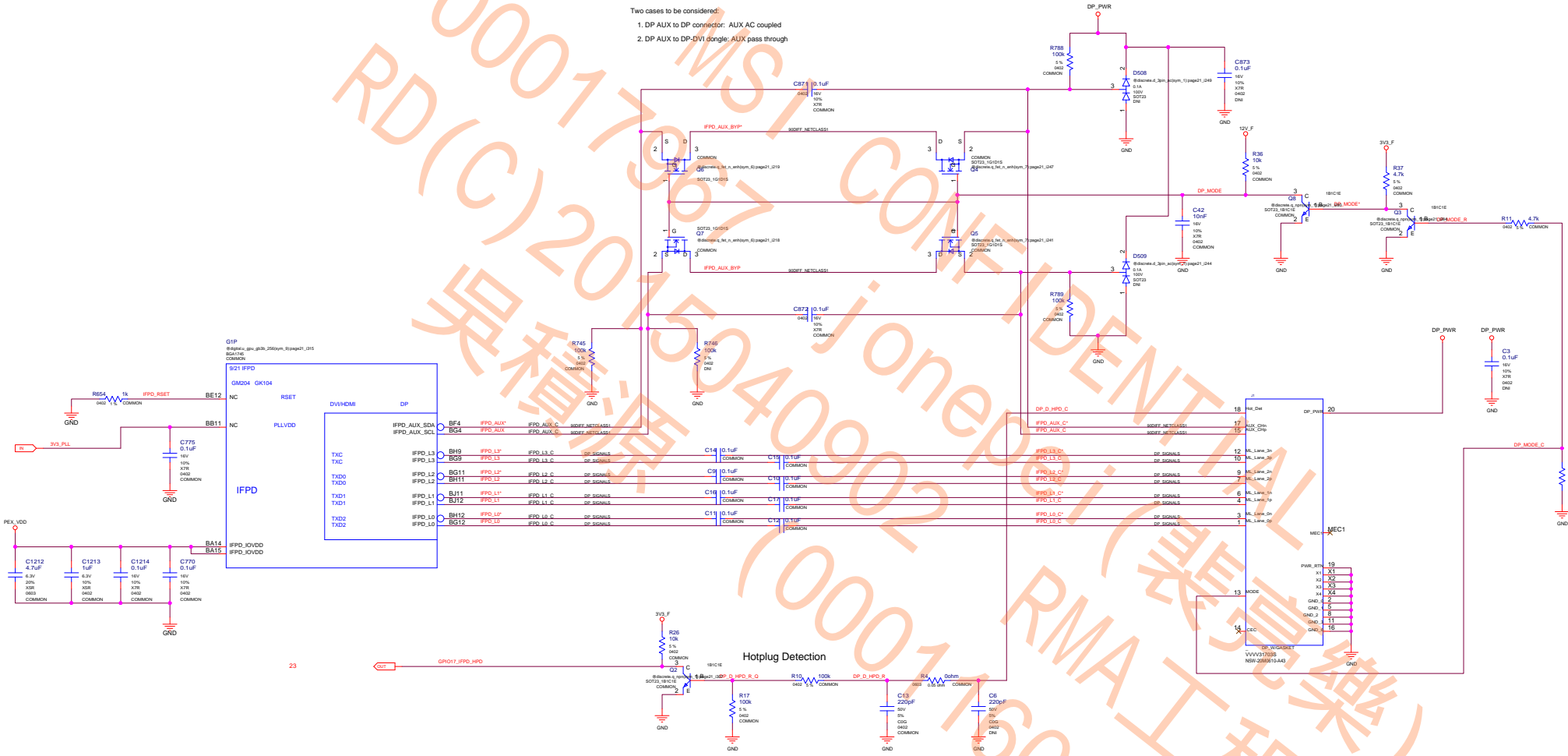
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Two cases to be considered:
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2. DP AUX to DP-DVI dongle: AUX pass through



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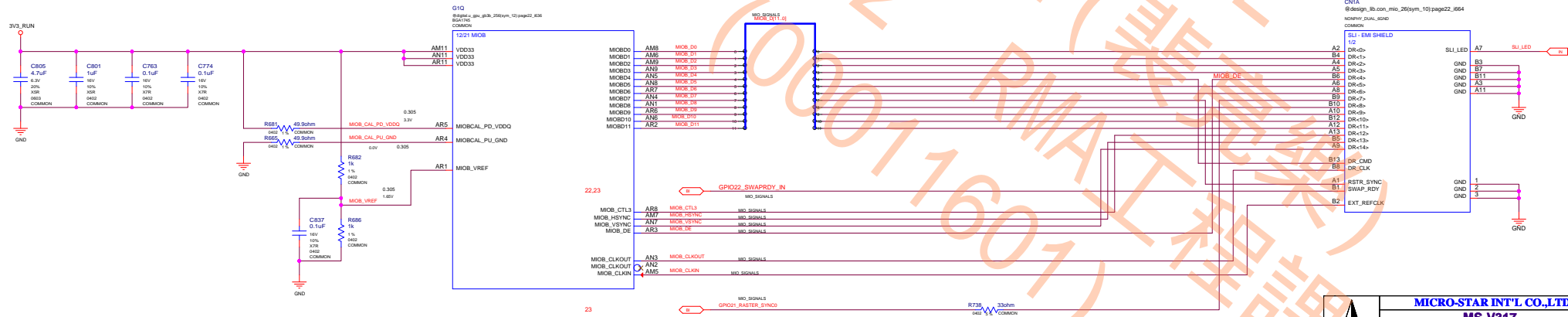
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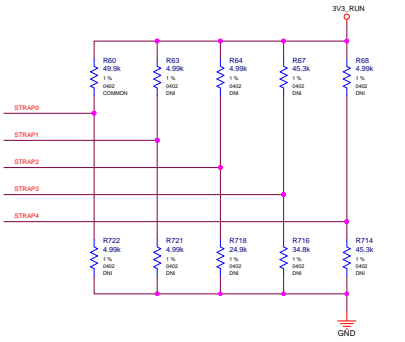
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STRAP0	KEPLER		
	USER_BIT [3:0]*	0000*	5K PD*
STRAP1	3GIO_PADCFG_LUT_ADR*	0000*	5K PD Overlap*
STRAP2	PCI_DEVID [3:0]*	0100 - (0x1184)*	25K PD - 45K GPU*
STRAP3	SOR_EXPOSED [3:0]*	1111*	45K PU*
STRAP4	DP_PLL_VDD_33V*	1*	FOR 3_3V*
	PEX_MAX_SPEED*	1*	FOR GEN2/3*
	PEX_SPD_CHANGE_GEN3*	1*	ENABLED*
	*		

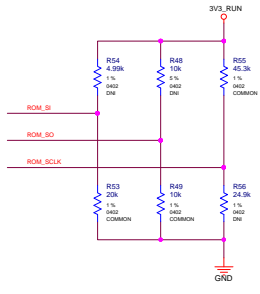
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	RAMCFG[1]*	1*	0111 for 64Mx32 256-bit SAMSUNG SAMSUNG for SKH2 0 primary memory
	RAMCFG[2]*	1*	45K PD*
	RAMCFG[3]*	0*	
ROM_SO	VGA_DEVICE*	1*	
	SMB_ALT_ADDR*	0*	30K PD*
	FB[0]_APERTURE_SIZE*	1*	For 128MB*
	FB[1]_APERTURE_SIZE*	0*	For 128MB*
ROM_SCLK	PEX_PLL_EN_TERM100*	0*	DISABLED*
	PCI_DEVID_EXT[5]*	0*	For 0x1184*
	SUB_VENDOR*	1*	Dedicated BIOS*
	PCI_DEVID_EXT[4]*	0*	For 0x1184*

MAXWELL		
GC6	SEE TABLE BELOW	
RAMCFG[0]*	1*	
	1*	20K PD*
	0*	
	0*	
VGA_DEVICE*	1*	
	0*	10K PD*
	0*	
	0*	
SOR0_EXPOSED*	1*	
	1*	45K PU*
	1*	
	1*	

MULTI_STRAP_REF0_GND	
BINARY PRODUCTION	NC
BINARY BRINGUP	NC
MULTI-LEVEL	45.3K 1% TO GND



MAXWELL		
STRAP0	3.3V	1.65V
STRAP1	1.65V	0V
STRAP2	0V	0V
STRAP3	0V	0V
STRAP4	0V	0V

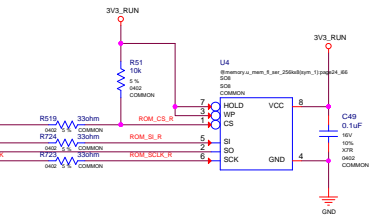
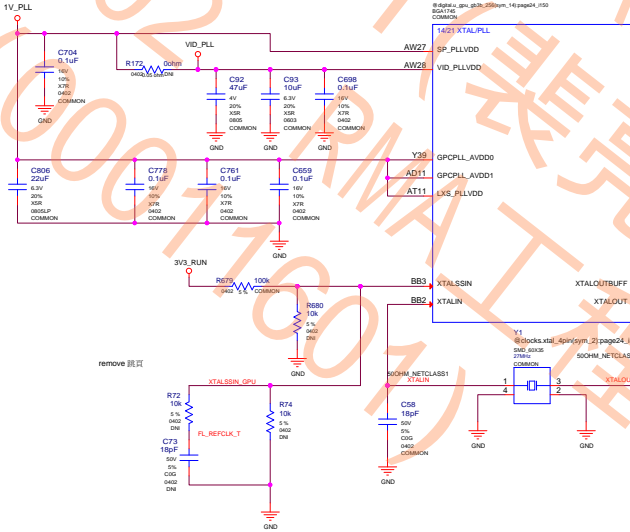


GND		
5K	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

CFG[3:0] Config Width Vendor		
0000	Reserved	
0001	32Mx32 256-bit Elpida	
0010	32Mx32 256-bit Hynix	
0011	32Mx32 256-bit Samsung	
0100	Reserved	
0101	64Mx32 256-bit Elpida	
0110	64Mx32 256-bit Hynix	
0111	64Mx32 256-bit Samsung	
1000	Reserved	
1001	32Mx32 192-bit Elpida	
1010	32Mx32 192-bit Hynix	
1011	32Mx32 192-bit Samsung	
1100	Reserved	
1101	64Mx32 192-bit Elpida	
1110	64Mx32 192-bit Hynix	
1111	64Mx32 192-bit Samsung	

CFG[3:0] Config Width Vendor		
0000	Reserved	
0001	128Mx32 256-bit Elpida	
0010	128Mx32 256-bit Hynix	
0011	128Mx32 256-bit Samsung	
0100	Reserved	
0101	64Mx32 256-bit Elpida	
0110	64Mx32 256-bit Hynix	
0111	64Mx32 256-bit Samsung	

0x13C0



Smart Fan

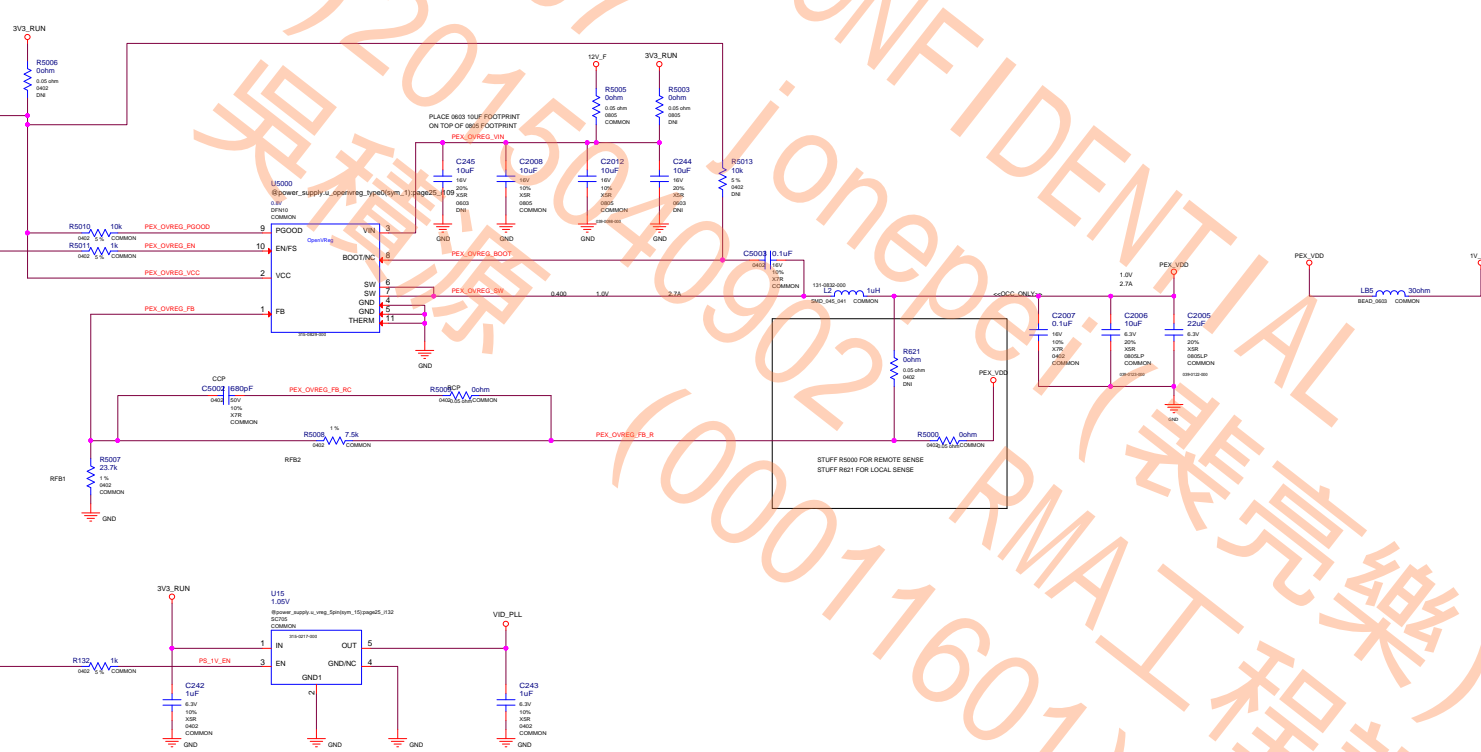
KEPLER		
XTALSSIN	XTALOUTBUFF	Inverted PWM %
PU	PU	66 (50% HIGH)
PD	PD	50 (50% HIGH)
PD	PU	33 (86% HIGH)
PD	PD	0 (100% HIGH)



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XTALOUTBUFF		
3.3V	1.65V	0V
66% PWM	33% PWM	DISABLED

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NV_PLN PCB REV BOM REV	600-10401-BASE-QS1 P-6017-A02 A		
	PAGE	25 OF 37	
	DATE	04-AUG-2014	

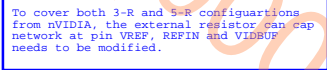
MSI CONFIDENTIAL
00017967 jonepei (裴亮樂)
RD(C)2015040902 RMA工程師
吳積源 (00011601)


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			MS-V317	
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Custom	NA			1.1
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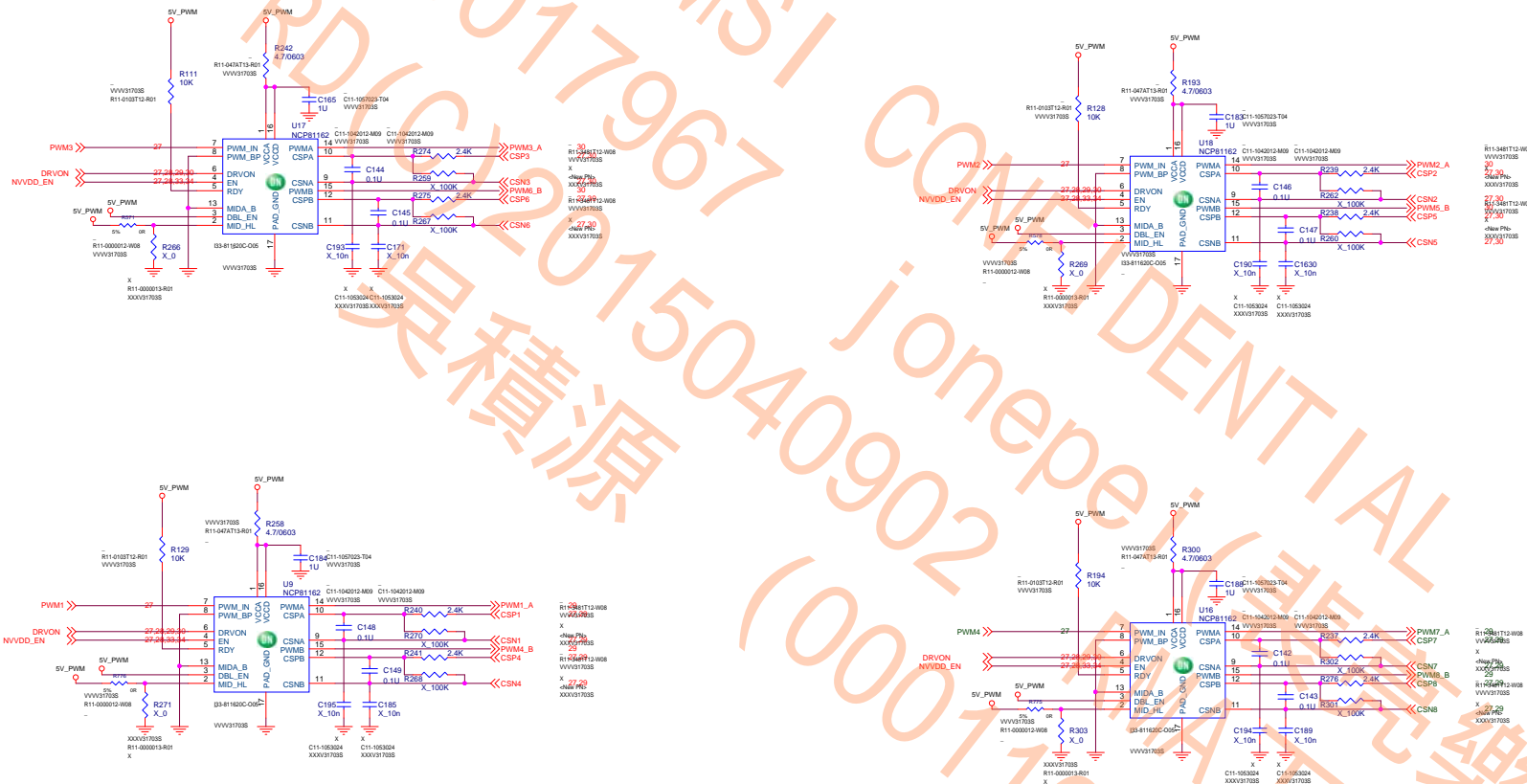
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BOX REV	A	DATE	04-AUG-2014



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DATE REV	BY	DATE	APPROVED BY

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: NVVDD Phase 1,2

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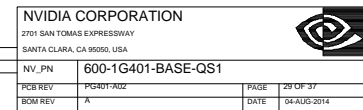
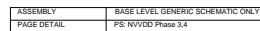
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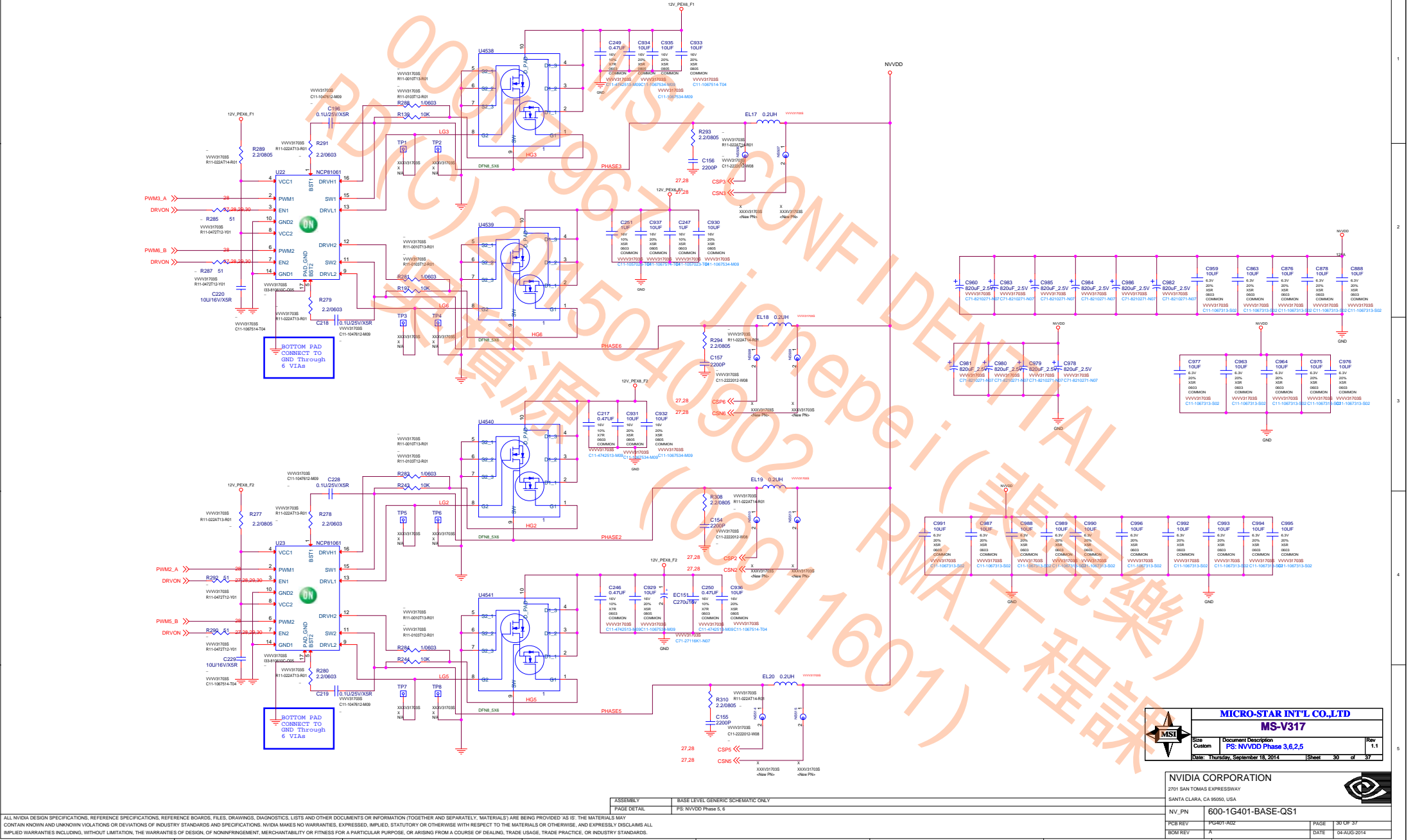
PG401-REV	PG401-ADZ	PAGE	28 OF 37
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DATE	04/05/2014
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Size Custom

Document Description PS: NVVDD Phase 3,6,2,5


Date: Thursday, September 16, 2014

Rev 1.1

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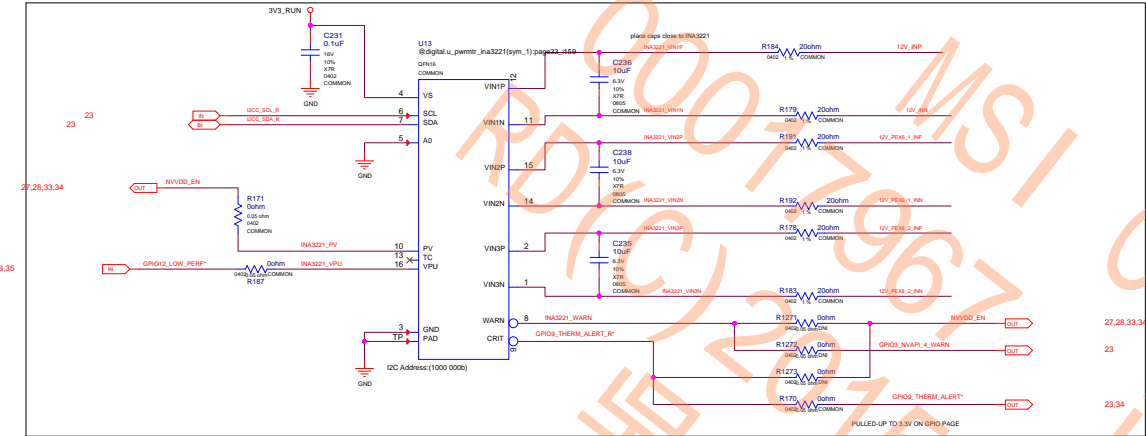
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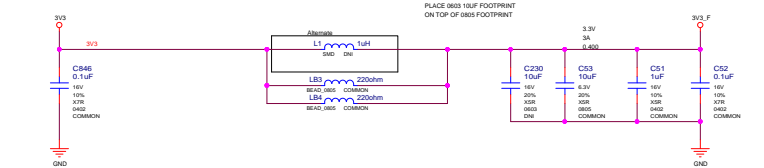
BOX REVA

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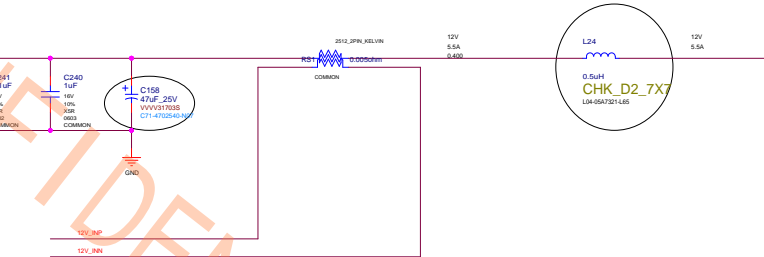
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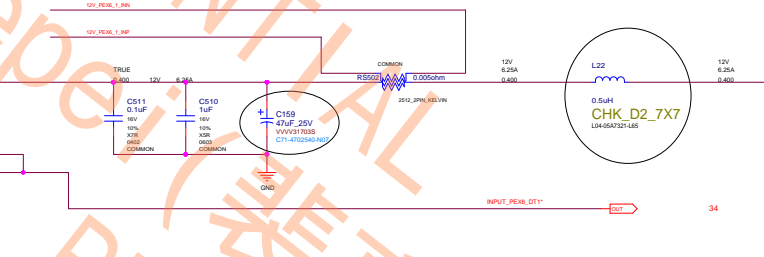
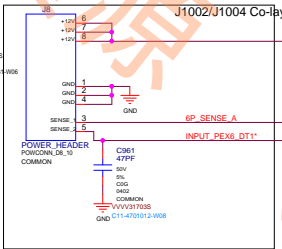
PEX 3V3 INPUT - 10W



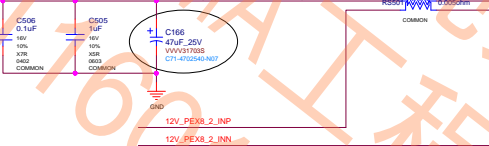
PEX_12V INPUT - 66W



PEX6 INPUT 1 - 2x3 PCIe CON 75W



PEX8 INPUT 2 - 2x4 PCIe CON 150W



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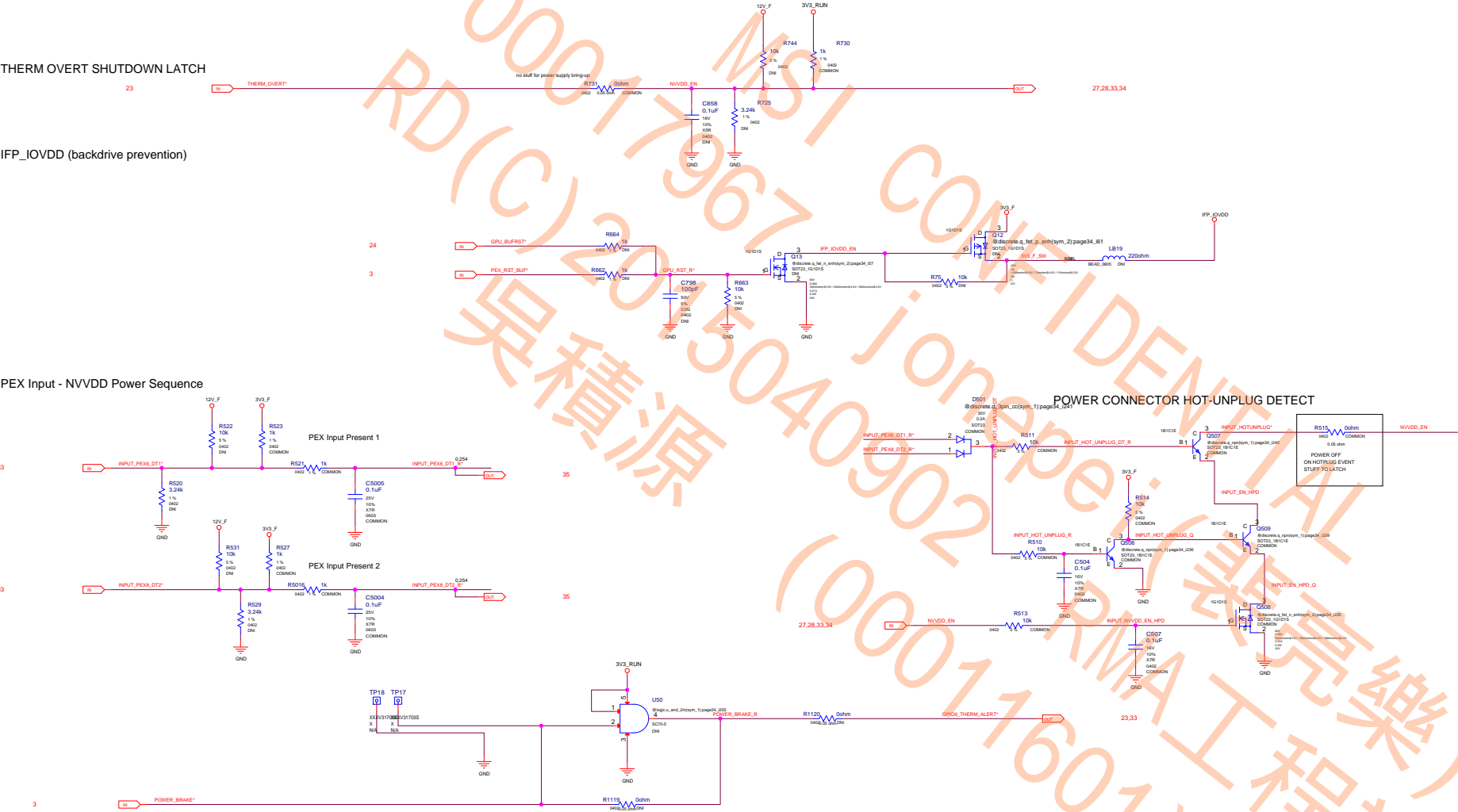
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: Inputs, Filtering, and Monitoring

THERM OVERT SHUTDOWN LATCH

IFP_IOVDD (backdrive prevention)

PEX Input - NVVDD Power Sequence



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: Shutdown

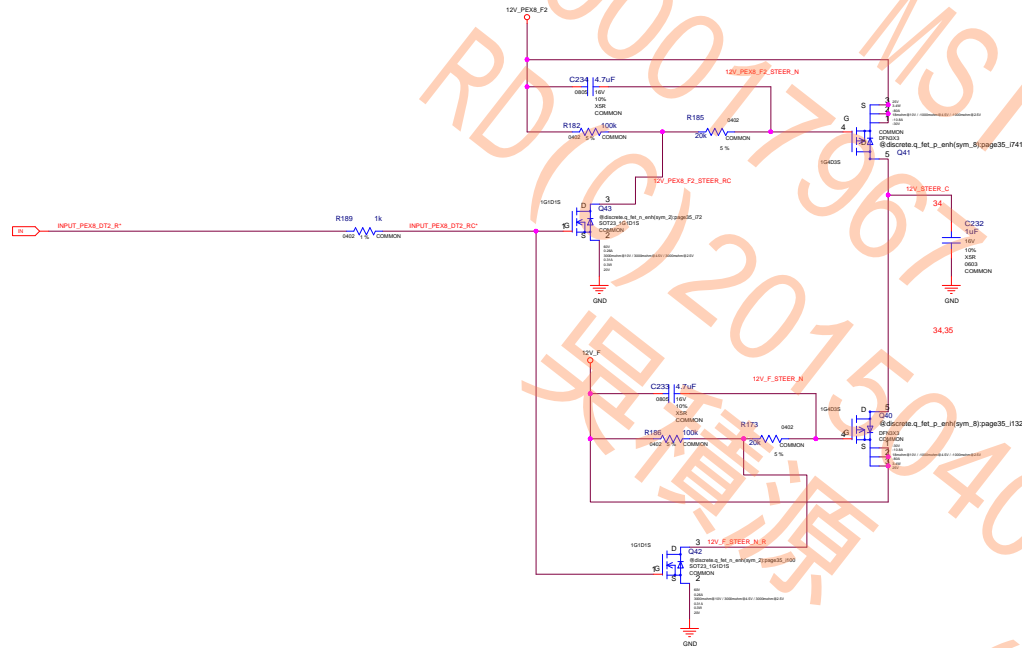
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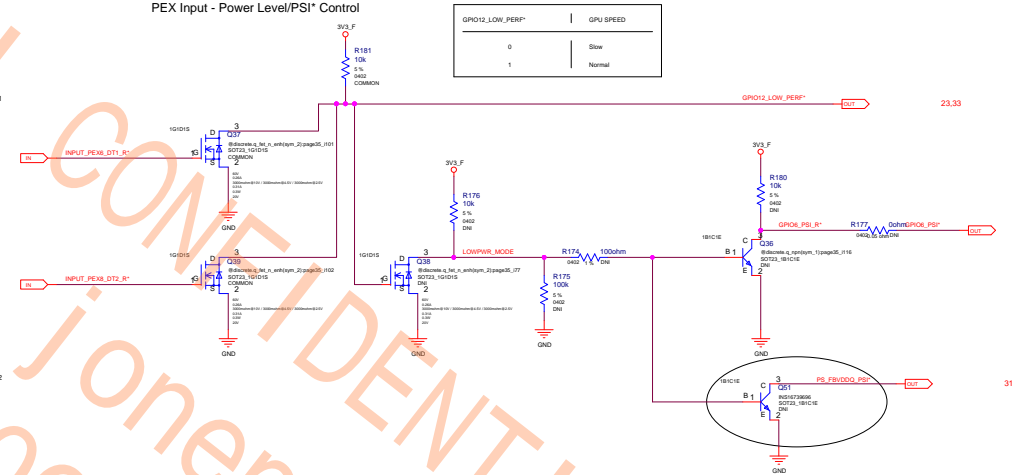
NV_PN	600-1G401-BASE-QS1
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PEX Input - 12V Current Steering FETs

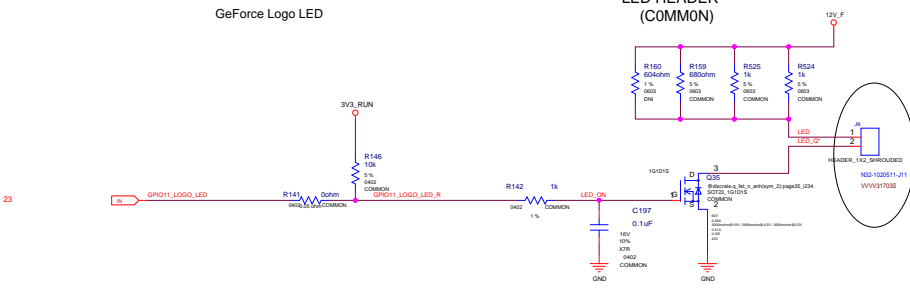


PEX Input - Power Level/PSI* Control

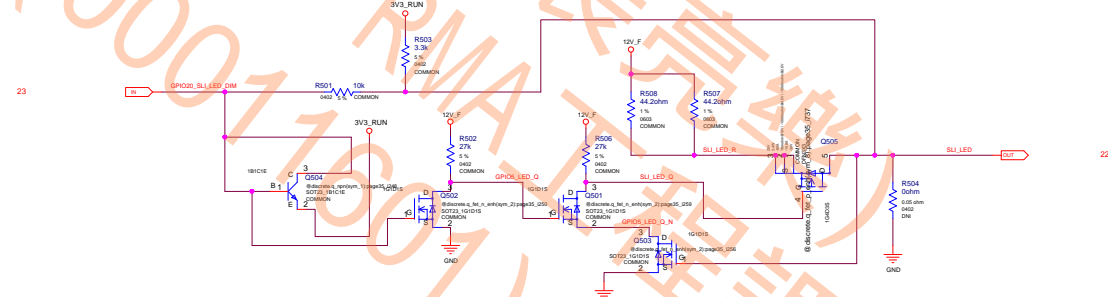


GeForce Logo LED

LED HEADER (COMMON)



SLI LED (GEFORCE ONLY)



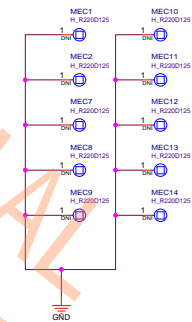
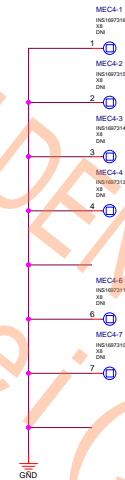
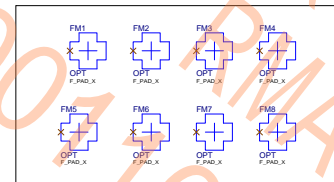
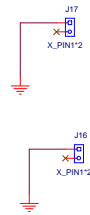
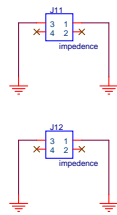
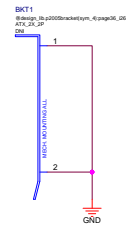
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- Page37:
- 1.P17 增加DVI ESD
 - 2.P18~P21 修改HDMI,DP footprint, 增加HDMI ESD
 - 3.简化S L I 線路
 - 4.移除原本FBVDDQ線路
 - 5.P27~P30 更換NVVD 線路
 - 6.P31~32 移除dynamic power circuit/增加風扇7511線路
 - 7.P33 更換反插8PIN,Input choke
 - 8.P35 增加MEM PSI 晶體
 - 9.Remove MICROCONTROLLER


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RD(C)2015040902
吳積源
jonepei (裴亮樂)
(00011601)
RMA工程師



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